Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.114”**

**SOURCE**

**GATE**

**.180”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: Source = .025” X .032”**

**Gate = .018” X .025”**

**Backside Potential: Drain**

**Mask Ref: HEX-3 GEN 3**

**APPROVED BY: DK DIE SIZE .114” X .180” DATE: 3/14/23**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC9130B**

**DG 10.1.2**

#### Rev B, 7/19/02